CERTIFICATE OF MAILING BY FIRST CLASS MAIL			Docket No. 351913-992800 (2102397-992800)
Applicant: EUGENE FENG			
Serial No. 10/643,622	Filing Date August 18, 2003	Examiner FAROOQ, MOHAMMAD O.	Group Art Unit 2181
Invention: MEMORY DEVICE OPERABLE WITH A PLURALITY OF PROTOCOLS			

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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission	16

Application Number	10/643,622
Filing Date	August 18, 2003
First Named Inventor	Eugene Feng
Art Unit	2181
Examiner Name	Farooq, Mohammad O.
Attorney Docket Number	351913-992800

ENCLOSURES *(Check all that apply)*

- ☒ Fee Transmittal Form
  - ☒ Fee Attached – $500
- ☐ Amendment/Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
  - ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
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- ☒ Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
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Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	DLA Piper Rudnick Gray Cary US LLP		
Signature	Ronald L. Yin		
Printed name	Ronald L. Yin		
Date	April 17, 2006	Reg. No.	27,607

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Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL for FY 2006

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($)500.00

Complete If Known	
Application Number	10/643,622
Filing Date	August 18, 2003
First Named Inventor	Eugene Feng
Examiner Name	Farooq, Mohammad O.
Art Unit	2181
Attorney Docket No.	351913-992800

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1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
		Small Entity		Small Entity		Small Entity	
Application Type	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims _____ - 20 or HP = _____ x Fee ($) _____ = Fees Paid ($) _____

HP = highest number of total claims paid for, if greater than 20

Indep. Claims _____ - 3 or HP = _____ x Fee ($) _____ = Fees Paid ($) _____

HP = highest number of independent claims paid for, if greater than 3

Multiple Dependent Claims Fee ($) _____ Fee Paid ($) _____

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets _____ - 100 = Extra Sheets _____ /50= Number of each additional 50 or fraction thereof _____ (round up to a whole number) x Fee ($) _____ = Fee Paid ($) _____

4. OTHER FEE(S)

	Fee Paid ($)
Non-English Specification, $130 fee (no small entity discount)	
Other (e.g., late filing surcharge): Filing of Appeal Brief	500

SUBMITTED BY

Signature	Ronald L. Yin	Registration No. 27,607 (Attorney/Agent)	Telephone (650) 833-2437
Name (Print/Type)	Ronald L. Yin		Date April 17, 2006

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

Eugene Feng

Application No. 10/643,622

Filed: August 18, 2003

For: MEMORY DEVICE OPERABLE WITH A PLURALITY OF PROTOCOLS

Group Art Unit: 2181

Examiner: Farooq, Mohammad O.

APPEAL BRIEF

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April 17, 2006

Rosa A. Caviedes

Rosa A. Caviedes

Dear Sir/Madam:

This is a brief for an appeal from a Final Office Action dated December 2, 2005, and from a Notice of Appeal that was filed on February 23, 2006.

TABLE OF CONTENTS

Real Party in Interest

The real party of interest is Silicon Storage Technology, Inc., pursuant to the assignment executed on August 15, 2003, and recorded on August 18, 2003 at reel 014415 and frame 0824.

Related Appeals and Interferences

There are no related appeals or interferences.

Status of Claims

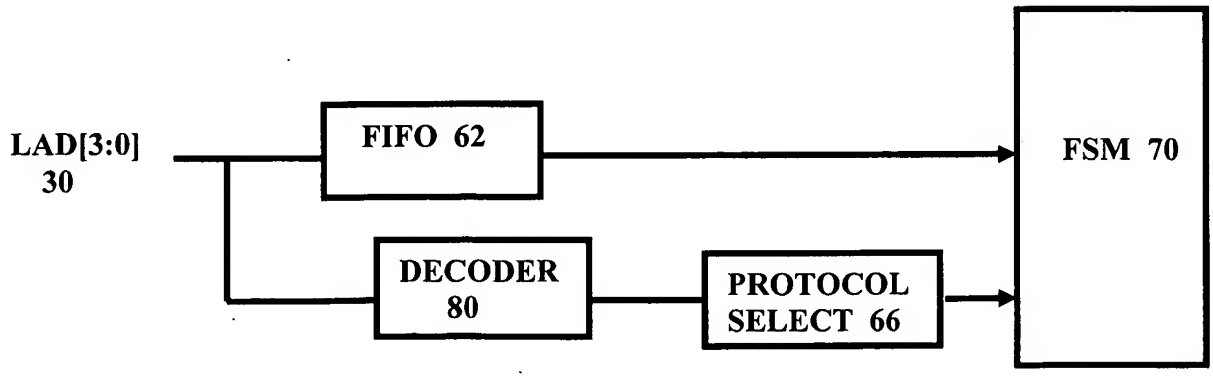
Claims 1-9 were originally presented on the filing of the application. This is an appeal of the rejected Claims 1-9.

Status of Amendments

No amendments were filed subsequent to final rejection.

Summary of Claimed Subject Matter

Applicants' invention, as claimed, deals with a memory device which interfaces with an integrated circuit communicating via a communication bus. An illustrative example of the device is shown in the application in Figure 4, reproduced hereinbelow.



As recited in claim 1, the memory device communicates via a communication bus which is shown as bus 30 in the drawing. The device comprises a decoding circuit which is shown as the decoder 80 which receives the communication signals via the communication bus 30. The decoder 80 decodes the communication signals and generates a plurality of protocol signals in response thereto. The protocol signals are supplied to the protocol select circuits 66. As stated in claim 1, "a protocol select circuit for receiving said plurality protocol signals." Thus, the output of the decoder circuit 80 is connected to the protocol select circuit 66. Claim 1 further recites an array of memory cells. This is not shown in Figure 4 but is shown as the memory 50 in Figure 3. Claim 1 further recites a controller circuit for controlling the operation of the array of memory cells. In Figure 4, the controller circuit is the finite state machine circuit 70. Finally, the protocol select circuit 66, configures the controller circuit 70 in response to the plurality protocol signals received from the decoder circuit 80. Thus, claim 1 as recited discloses a decoder circuit 80 connected to the communication bus 30 for receiving communication signals therefrom, and generates signals that are supplied to the protocol select circuit 66 which processes those signals and supplies them to the finite state machine circuit 70, which then controls the memory array

Grounds of Rejection to be Reviewed on Appeal

The grounds of rejection to be reviewed on appeal are as follows:

1. Whether claim 1 was properly rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,805,931 ("Morzano et al.") in view of U.S. Patent 5,367,646 ("Pardillos et al.")

2. Whether claims 2-8 were properly rejected under 35 U.S.C. 103(a) as being unpatentable over Morzano et al. in view of Pardillos et al. further in view of U.S. Patent 6,542,391 ("Pereira et al.")

3. Whether claim 9 was properly rejected under 35 U.S.C. 103(a) as being unpatentable over Morzano et al. in view of Pardillos et al. and Pereira et al. and further in view of U.S. Patent 6,188,602 ("Alexander et al").

Argument

1. Claim 1 was Improperly Rejected under 35 U.S. §103(a) as being unpatentable over Morzano et al. in view of Pardillos et al.

In the final rejection, the examiner alleged that Morzano taught Applicant's invention as set forth in claim 1 in the following manner:

A decoding circuit is set forth in item 378, Figure 10 of Morzano; a protocol select circuit is shown by the controller circuit described in col. 14, lines 8-23; an array of memory cells is shown by the SAMs, as described in col. 14, lines 8-23; and the protocol select circuit for configuring the controller circuit in response to the plurality of protocol signals is shown in Fig. 7-13, col. 14, lines 8-23. According to the examiner: "Morzano et al. do not teach a control circuit for controlling the operation of said array of memory cells. Pardillos et al. teach a control circuit for controlling the operation of said array of memory cells (i.e. memory access controller; col. 21, line 50 - col. 22, line 29). However, it would have been obvious to one of ordinary skill in the art at the time of invention to combine the teachings of Morzano et al. and Pardillos et al. because that would provide the best use of microprocessor performance wherein it would not be limited by the existence of only one bus (col. 3, lines 65 – col. 4, line 7)."

As discussed above, Applicant's invention as claimed describes the interconnection of a number of elements in a specified manner. For example, the decoding circuit 80 receives communication signals from the bus 30 and generates a plurality of protocol signals which are supplied to a protocol select circuit 66, which in turn configures the controller circuit 70, which controls the operation of an array of memory cells.

According to the examiner, the decoder circuit of applicant's invention as claimed is met by the element 378 shown in Figure 10. Further, according to the Examiner, the protocol circuit of applicant's invention as claimed is met by the controller circuit shown in col. 14, lines 8-23 of Morzano et al. However, a reading of Morzano et al. shows that nowhere is the decoder 378 specifically mentioned in col. 14, lines 8-23. What is mentioned instead is that "[E]ach of the SAMs 502, 504... 510 receives decode signals from a respective decoder 542, 544...550 which, in turn, receive appropriate signals from a respective controller circuit 562, 564... 570." The controller circuit 562, 564 ...570, however, is shown in Fig. 14. It is shown as supplying signals **TO** a SAM 0 decoder, which is shown in Figure 10, of which decoder 378 is a part thereof. Thus, contrary to Applicant's invention as claimed, Morzano et al. does not teach a decoder receiving a bus signal and generating decoded signals and SUPPLYING the decoded signal to a protocol select circuit. Instead, in Morzano et al. it appears the controller circuit supplies signals to a decoder circuit.

The Examiner further conceded that Morzano does not disclose a control circuit for controlling the operation of said array of memory cells. However, according to the Examiner, this is met by the memory access controller; col. 21, line 50 - col. 22, line 29 of Pardillos et al. Applicant respectfully submits that even if it were obvious to combine Morzano et al. and Pardillos et al., (an assumption not concede by applicant) the resultant combination would still

not result in applicant's invention as claimed in two significant manner: 1) as previously discussed, the combination still does not disclose a protocol circuit which receives signals from a decoder circuit; and 2) the Examiner has failed to demonstrate how the controller circuit of Pardillos et al. is configured by the protocol select circuit as claimed in applicant's claim 1.

In response to applicant's arguments, the examiner stated that "the rejection is an obviousness rejection not an anticipation rejection" What the examiner fails to note is that even in an obviousness rejection, using a combination of references, the combination must teach all of the claimed elements connected in the manner recited in the rejected claim. In this case, the combination of Morzano et al. and Pardillos et al. fails to show the interconnection of the claimed elements, as recited in claim 1.

2. Claims 2-8 were Improperly Rejected under 35 U.S. §103(a) as being unpatentable over Morzano et al. and Pardillos et al. in view of Pereira et al.

In the final rejection, the examiner rejected claims 2-6 and alleged that Morzano et al. and Pardillos et al. taught Applicant's invention as set forth in claim 1 but that neither Morzano et al. nor Pardillos et al taught non-volatile storage element, and that Morzano taught volatile storage element, and that Pereira et al. taught non-volatile storage element.

Applicant respectfully submits that since claims 2-6 are dependent upon claim 1, the same shortcomings of the combination of Morzano et al. with Pardillos et al. is not overcome by the addition of the reference Pereira et al. In particular, the combination of Morzano et al. with Pardillos et al. and Pereira et al. does not disclose the claimed limitations of a decoding circuit generating a plurality of protocol signals which are supplied to a protocol select circuit, which configures a controller circuit, which controls the operation of an array of memory cells.

With respect to claim 7, which is an independent claim, and which recites a more limiting feature of claim 1, namely that the communication signal is in the LPC protocol, the Examiner also rejected claim 7 based upon the combination of references Morzano et al. with Pardillos et al. and Pereira et al. Similar to claim 1, claim 7 also recites the interconnection of a number of elements in a specified manner. For example, the decoding circuit receives the start field of an LPC signal and generates a plurality of protocol signals which are supplied to a protocol select circuit, which configures the controller circuit, which controls the operation of an array of memory cells.

As with the rejection of claim 1 based upon the combination of Morzano et al. with Pardillos et al, the Examiner failed to recognize that the combination of references Morzano et al. with Pardillos et al. and Pereira et al. does not disclose the interconnection of a number of claim elements in a specified manner, such as, the decoding circuit, receiving the start field of an LPC signal and generating a plurality of protocol signals which are supplied to a protocol select circuit, which configures the controller circuit, which controls the operation of an array of memory cells. Furthermore, the combination of Morzano et al. with Pardillos et al. and Pereira et al. also does not teach processing of an LPC communication signal in the manner set forth in claim 7. In fact, the Examiner's rejection appears to be "canned" in that the Examiner stated "Pereira et al teach non-volatile memory (col. 18, lines 17-25)." However, nothing in claim 7 recites a non-volatile memory.

With respect claim 8, which is dependent upon claim 7, applicant respectfully submits that the same shortcomings of the combination of Morzano et al. with Pardillos et al. is not overcome by the addition of the reference Pereira et al. In particular, the combination of Morzano et al. with Pardillos et al. and Pereira et al. does not disclose the claimed limitations of

a decoding circuit generating a plurality of protocol signals which are supplied to a protocol select circuit, which configures a controller circuit, which controls the operation of an array of memory cells.

Thus, applicant respectfully submits that the claims 2-8 were improperly rejected by the combination of Morzano et al. with Pardillos et al. and Pereira et al.

3. Claim 9 was Improperly Rejected under 35 U.S. §103(a) as being unpatentable over Morzano et al., in view of Pardillos et al., and Pereira et al. and further in view of Alexander et al.

In rejecting claim 9, which depends upon claim 7, the Examiner conceded that the combination of Morzano et al., in view of Pardillos et al., and Pereira et al. do not teach protocol for LPC communication and for FWH communication. According to the examiner, Alexander et a. teach protocol for LPC communication and for FWH communication.

However, as before the combination of Morzano et al., in view of Pardillos et al., and Pereira et al. and further in view of Alexander et al. still fails to teach the interconnection of a number of elements in a specified manner, such as, the decoding circuit, receiving the start field of an LPC signal and generating a plurality of protocol signals which are supplied to a protocol select circuit, which configures the controller circuit, which controls the operation of an array of memory cells.

Therefore, for this reason, the rejection of claim 9 based upon the combination of Morzano et al. in view of Pardillos et al. and Pereira et al. and further in view of Alexander et al. is improper.

Conclusion

For all of the reasons set forth hereinabove, Applicants respectfully submit that the claims appended hereto are patentable and urge a reversal of the final rejection.

Respectfully submitted,

DLA Piper Rudnick Gray Cary US LLP

Dated: April 17, 2006

By: Ronald L. Yin

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Appendix

1. A memory device for interfacing with an integrated circuit communicating via a communication bus, said device comprising:

a decoding circuit for receiving communication signals received via the communication bus, for decoding the communication signals and for generating a plurality of protocol signals in response thereto;

a protocol select circuit for receiving said plurality of protocol signals;

an array of memory cells;

a controller circuit for controlling the operation of said array of memory cells;

said protocol select circuit for configuring the controller circuit in response to the plurality of protocol signals.

2. The device of claim 1 wherein said memory cells are non-volatile memory cells.

3. The device of claim 2 wherein said protocol select circuit is a volatile storage element.

4. The device of claim 3 wherein said volatile storage element is a register.

5. The device of claim 3 wherein said volatile storage element is a flip-flop.

6. The device of claim 3 wherein said volatile storage element is an SRAM.

7. A memory device for interfacing with an integrated circuit communicating via an LPC bus, said circuit generating a start field, said device comprising:

a decoding circuit for receiving the start field and for generating a plurality of protocol signals;

a protocol select circuit for receiving said plurality of protocol signals;

an array of non-volatile memory cells;

a controller circuit for controlling the operation of said array of non-volatile memory cells;

said protocol select circuit for configuring the controller circuit in response to the plurality of protocol signals.

8. The device of claim 7 wherein said protocol select circuit is a flip-flop.

9. The device of claim 7 wherein said plurality of protocol signals represent protocol for LPC communication and for FWH communication